

PATENT APPLICATION

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Inventor(s): Tien M. Nguyen, James Yoh,
Ashok Mathur, & Gary W. Goo

Title: Random Walk Filter Timing Recovery Loop

SPECIFICATION

Statement of Government Interest

The invention was made with Government support under contract No. F04701-00-C-0009 by the Department of the Air Force. The Government has certain rights in the invention.

Field of the Invention

The invention relates to the field of digital communications. More particularly, the present invention relates to timing recovery loops for accurate detection and tracking of binary data streams.

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Background of the Invention

In a communication receiver, a received RF signal is demodulated to generate a baseband signal waveform containing a self-clocking bit stream of digital data. The baseband signal waveform is tracked using a timing recovery loop. The timing recovery loop tracks bit timing of the baseband signal waveform and generates timing pulses, which are then used in a data detector for sampling the baseband signal waveform at the bit intervals for reconstructing the digital bit stream from the received baseband signal waveform. The baseband signal waveform is subject to channel noise leading to poorly generated timing pulses and hence poor bit timing resulting in poor data detection. When the timing recovery loop loses track, the bit stream is no longer detected. The bit stream is recovered using conventional timing recovery loops that are subject to bit timing lock drop in the timing recovery loop.

The conventional timing recovery loops use early-and-late gates, digital transition tracking, filter-and-square, and delay-and-multiply functions. In bit timing detection, the bit stream is self clocking and the timing differential dithers about correct bit timing in the timing recovery loops. For mobile environments, these timing recovery loops drop lock when the loop signal-to-noise ratio (SNR) is smaller than a threshold value or the residual Doppler frequency is larger than the operating loop bandwidth. Timing recovery loops use

1 slow bandwidth phase lock loops that drop lock at low SNR.
2 After dropping lock, the conventional timing recovery loops
3 disadvantageously experience long hang up time due to the need
4 to reacquire the timing pulses.

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6 Random walk filters have been used for decades in various
7 applications. In the past, random walk filters have been
8 applied to digital phase synchronization systems. Random walk
9 filters have been theoretically applied to carrier phase
10 detection where differentials between local references and
11 transmitter carriers results in a phase correction that is
12 unidirectional and constantly circular over 360 degrees.
13 Although used for decades, random walk filters have not been
14 adapted to improving the bit clock locking stability in timing
15 recovery loops. Random walk filters have not been applied to
16 recover bit timing information of a digital data stream.
17 Existing timing recover loops suffer from drop of bit timing
18 lock in noisy channels. Noisy channels suffer from ambiguous
19 bit timing transitions leading to jittering and inaccurate
20 timing pulses. These and other disadvantages are solved or
21 reduced using the invention.

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Summary of the Invention

An object of the invention is to provide improved detection of a binary data stream encoded in a baseband signal.

Another object of the invention is to provide a timing recovery loop with a random walk filter counter for maintaining bit timing lock of a binary signal waveform.

Yet another object of the invention is to provide a timing recovery loop with a random walk filter counter counting early and late transitions of an input baseband binary signal waveform for adjusting generated timing pulses to the actual bit timing of the baseband binary signal waveform.

Still another object of the invention is to provide a timing recovery loop with a random walk filter counter counting early and late transitions of an input baseband binary signal waveform for adjusting generated timing pulses to the actual bit timing of the baseband binary signal waveform, and, with a threshold selector, determine when the accumulated early and late transitions exceed a predetermined threshold value for adjusting the generated timing pulses.

A further object of the invention is to provide a timing recovery loop with a random walk filter counter counting early and late transitions of an input baseband binary signal

1 waveform for adjusting the generated timing pulses to the
2 actual bit timing of the baseband binary signal waveform, and,
3 with a threshold selector, determine when the accumulated early
4 and late transitions exceed a predetermined threshold value for
5 adjusting the generated timing pulses, with the threshold value
6 being dynamically adjusted.

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8 The invention is directed to a timing recovery loop
9 enhanced with a random walk filter. The enhanced timing
10 recovery loop achieves improvement in reduced timing jitter. A
11 setable error threshold enables adaptive synchronization in the
12 timing recovery loop, reduces drop lock rates and decreases the
13 acquisition time. The dropped-lock rate is less frequent due to
14 the setting of the threshold value of the random walk filter
15 timing recovery loop. The threshold value can be adaptively
16 reset. The random walk filter timing recovery loop provides
17 faster acquisition time by adaptively setting the threshold
18 value to changing channel environments. As an example, the
19 threshold value can be based on the frequency of the
20 adjustments to the generated timing pulses so as to provide
21 responsive and yet not overly jittery adjustments.

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1 An input baseband signal waveform containing a digital bit
2 stream is detected to generate data transition pulses that are
3 compared in time with locally generated and suitably delayed
4 timing pulses to produce lead and lag signals to respectively
5 increment and decrement a random walk filter timing counter.
6 When the random walk filter timing counter output exceeds a
7 positive or negative threshold, the delay for timing pulses is
8 respectively adjusted in time forwards or backwards according
9 to the sign of the exceeded threshold. With a stable input
10 binary signal waveform, with accurate timing, and in a low
11 noise channel, for example, an appropriately selected threshold
12 value allows the lead and lag signals to cancel out in time,
13 thus allowing the generated timing pulses to remain
14 synchronized to the input binary signal waveform without delay
15 adjustments. In noisy channels or with a Doppler shifted input
16 signal, the input binary signal waveform skews in time. As the
17 input binary signal waveform skews in early or late time
18 relative to the generated timing pulses, the respective lead
19 and lag signals accumulate over time, and when exceeding a
20 threshold number, the generated timing pulses are adjusted
21 early or late in relative time for improved tracked
22 synchronized timing with the input binary signal waveform, so
23 as to maintain bit timing lock. As such, the random walk filter
24 continuously adjusts the generated timing pulses to maintain an
25 accurate bit timing lock.

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27 The timing recovery loop can be implemented with low power
28 digital technology and is applicable to a wide range of

modulation schemes that are well suited for enhanced mobile communications. The random walk filter timing recovery loop is expandable to accommodate a wide range of amplitude and phase modulation schemes, such as, BPSK, QPSK, GMSK, 16-QAM, and 64-QAM. These and other advantages will become more apparent from the following detailed description of the preferred embodiment.

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Brief Description of the Drawings

Figure 1 is a block diagram of a random walk filter timing recovery loop.

Figure 2 is a process flow diagram of a pulse detector and comparator.

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Detailed Description of the Preferred Embodiment

An embodiment of the invention is described with reference to the figures using reference designations as shown in the figures. Referring to Figure 1, a baseband signal waveform 10 carries an input digital bit stream of encoded data. The binary data and timing are encoded into the baseband signal waveform 10. The baseband signal waveform 10 is fed into a conventional data detector 11 and a pulse detector and comparator 12. The pulse detector and comparator 12 generates adjusted timing pulses 14 that can be used by the data detector 11 to sample the baseband signal waveform 10 to reconstruct the digital bit stream 15. The baseband signal waveform 10 has been carrier-demodulated.

The pulse detector and comparator 12 receives the baseband signal waveform 10 and generates the adjusted timing pulses 14. The data may be encoding onto the baseband signal in several different types of formats, such as binary pulse shift keying (BPSK). For example, BPSK encoding has zero crossings as transitions that may indicate bit timing with maxima and minima indicating binary ones and zeros, respectively. The pulse detector and comparator 12 detects the zero crossing transitions, generates data transition pulses, and compares the generated data transition pulses with the adjusted timing pulses that will be adjusted from time to time to allow for changes in the input baseband signal waveform over time during

reception. The adjusted timing pulses 14 are adjusted to follow the data transition pulses for continuous reliable data detection by the data detector 11, resulting in a reconstructed digital bit stream 15 with a low error rate. The pulse detector and comparator 12 generates the data transition pulses from the baseband signal waveform 10 and compares the data transition pulses with the timing pulses for determining early, nominal and late arrivals of the data transition pulses relative to the timing pulses. Based on the comparison between the data transition pulses and adjusted timing pulses, -1 lead, 0 nominal, and +1 lag outputs are generated indicating the time relationship between the adjusted timing pulses and data transition pulses.

A random walk filter counter 16 receives lead, nominal, and lag outputs from the pulse detector and comparator 12 and generates a running count that is incremented, maintained, or decremented respectively by the lead, nominal, and lag outputs. The running count is fed to count magnitude generator 18 and a count sign clipper 20. The magnitude generator 18 generates a magnitude count that is fed to a threshold comparator 22, which receives a threshold value from a threshold value selector 24. The threshold value is a predetermined selected threshold value that can be changed in the face of different operating conditions. The threshold comparator 22 provides an input to the threshold value selector 24 for adaptive threshold selection preferably based on the rate at which the threshold value is exceeded. The magnitude count is the magnitude of the

1 running count. The count sign clipper 20 provides a plus or
2 minus count sign to a timing pulse delay adjustor 26. The count
3 sign is the sign of the running count from the random walk
4 filter counter 16. The threshold comparator 22 compares the
5 magnitude count with a threshold value selected by a threshold
6 value selector 24.

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8 The threshold comparator 22 generates an exceeded signal
9 when the magnitude count of the running count from the
10 magnitude generator 18 is greater than the selected threshold
11 value. The threshold comparator 22 communicates the exceeded
12 signal to the timing pulse delay adjustor 26. The count sign
13 clipper 20 generates the count sign indicating the early or
14 late timing of the magnitude count. When the running count
15 exceeds the threshold value, and an exceeded signal is sent to
16 the timing pulse delay adjustor 26, an additional timing delay
17 adjustment is made in the generation of the adjusted timing
18 pulses 14 in the pulse detector and comparator 12, which
19 outputs the adjusted timing pulses 14 for data detection. The
20 timing pulse delay adjustor 26 uses the count sign of the
21 running count to adjust early and late in time by a fixed time
22 period, resulting in an adjusted timing pulse delay 28 that is
23 communicated to the pulse detector and comparator 12 that then
24 appropriately adjusts the adjusted timing pulses 14 and then
25 outputs the adjusted timing pulses 14. The early and late
26 timing adjustment is made when triggered by the exceeded
27 signal. The early and late timing adjustment to the adjusted
28 timing pulses is in such a direction as to reduce the time

1 difference between the adjusted timing pulses 14 and the data
2 transition pulses of the baseband signal waveform 10.

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4 The threshold value selector 24 preferably adaptively
5 selects the threshold value depending on the channel
6 environment. Either a training sequence or apriori knowledge
7 of the channel propagation conditions can be used to initially
8 set the threshold value to an initial threshold value. As the
9 channel experiences excessive noise or continuous gross change
10 in the actual bit timing, the threshold value comparator 22 can
11 keep track of the rate at which the magnitude count exceeds the
12 threshold, that is the rate of timing adjustments, and in the
13 case of a low rate of magnitude counts exceeding the threshold
14 value, resulting in few timing adjustments, the threshold
15 comparator 22 can signal the threshold value selector 24 to
16 select the next lower threshold value, or, in the case of a
17 high rate of magnitude counts exceeding the threshold value,
18 resulting in many timing adjustments, such as in the presence
19 of excessive noise, the threshold comparator 22 can signal the
20 threshold value selector 24 to select the next higher threshold
21 value. In this manner, the threshold value is adaptively
22 adjusted to be lower and higher by the threshold value selector
23 24, corresponding to channel conditions and changes to the
24 actual bit timing.

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Referring to Figures 1 and 2, and more particularly to Figure 2, the pulse detector and comparator 12 receives the adjusted timing pulse delay 28 from the timing pulse delay adjustor 26, and receives the baseband signal waveform 10 and provides the +1 lead, 0 nominal, and -1 lag signals to the random walk filter counter 16. The data transition pulses are generated 30 from the baseband signal waveform 10. The generation of the data transition pulses depends on the type of modulation used to communicate the encoded digital bit stream in the baseband waveform 10. The data transition pulses can be, for example, generated at each zero crossing of the baseband signal waveform, such as when using BPSK modulation. The baseband signal waveform 10 with BPSK modulation has transitions from plus one to minus one and from minus one to plus one. A transition pulse is generated at the time of zero crossing when a transition occurs. During a bit interval, no transition pulse, more than one transition pulse, but most often, only one transition pulse is generated.

The generated 30 data transition pulses are then delayed 32 by half of a search window size W . A window size W is typically the data bit period, but smaller search windows could also be used as long as there is a high probability that the data transition pulses are found within the windows. The $W/2$ delay 32 shifts the time of the data transition pulses to the center of a search window under ideal conditions, with the search window starting from an adjusted timing pulse. The search window size allows a data transition pulse to be

1 detected under conditions that are not ideal, as the baseband
2 signal waveform 10 is subject to noise causing the data
3 transition pulse to randomly shift in time within the search
4 window causing bit timing mismatches. Doppler shifts can also
5 skew the data transition pulses. The random walk filter timing
6 recovery loop serves to continuously adjust in time by the
7 adjusted delay the adjusted timing pulses to be synchronized
8 with the data transition pulses for improved bit timing
9 tracking and consequently improved data detection by the data
10 detector 11.

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12 The baseband signal waveform 10 is used to generate the
13 data transition pulses 30 delayed by half of the search window
14 size, $W/2$. Reference timing pulses are generated 36 typically
15 by a local oscillator, not shown, providing a digital clocking
16 reference. The reference timing pulses are set to the expected
17 bit clocking rate of the encoded digital bit stream of the
18 baseband waveform 10 so as to match in time under ideal
19 condition the adjusted timing pulses to the expected data
20 transition pulses. The reference timing pulses are effectively
21 shifted 34 in time by the adjusted timing pulse delay 28 from
22 the timing pulse delay adjustor 26 to generate the adjusted
23 timing pulses 14.

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25 The number of data transition pulses within the search
26 window W from an adjusted timing pulse are counted 38. The
27 number of data transition pulses can be zero, one, or more than
28 one. When determined 40 that the number of data transition

1 pulses within the search window is not equal to one, there is
2 insufficient or ambiguous information to indicate early or late
3 arrival of the data transition pulse within the search window
4 W , and the zero nominal lag signal is output 42 so that the
5 random walk filter counter 16 does not increment nor decrement
6 the running count. When the number of data transition pulses 40
7 is equal to one, then the lead or lag time between the adjusted
8 timing pulse and the $W/2$ delayed data transition pulse is
9 calculated 44. The calculated lead or lag time of arrival of
10 the delayed data transition pulse is clipped 46 into a minus
11 one early or plus one lag time, and a +1 lead or a -1 lag
12 signal generated 48 and output 50 to the random walk filter
13 counter 16. The data transition counting 44 counts number of
14 data transition pulses that are within search window W from
15 each successive timing pulse, and keeps track of the location
16 of the first data transition pulse within the search window.
17 The lead or lag time is calculated 44 for the first data
18 transition pulse only as the pulse location in the search
19 window minus half of the search window size. The lead and lag
20 outputs 50 is presented when there is one, and only one, data
21 transition pulse within the search window, thus reducing noise
22 related ambiguity in the bit timing tracking. In this manner,
23 the pulse detector and comparator 12 continuously increases or
24 decreases the timing pulse delay from the timing pulse delay
25 adjustor 26 to maintain synchronization between the adjusted
26 timing pulses 14 and the baseband signal waveform 10.

1 The present invention uses a random walk filter counter in
2 a digital timing recovery loop for reducing the drop lock rate
3 by setting a threshold value in a timing recovery loop. The
4 enhanced timing recovery loop offers faster acquisition time
5 due to the threshold value setting that can be made adaptive to
6 the channel environment. The timing recovery loop can be
7 implemented using conventional digital technology for low costs
8 and can use low sampling rates to reduce power usage. The
9 timing recovery loop is applicable to a wide range of
10 communication modulation methods, such as BPSK, QPSK, 16-QAM,
11 64-QAM, and GMSK. The random walk filter timing recovery loop
12 can be applied to wireless communications such as cellular
13 phones, mobile phones, and satellite decoders. Those skilled in
14 the art can make enhancements, improvements, and modifications
15 to the invention, and these enhancements, improvements, and
16 modifications may nonetheless fall within the spirit and scope
17 of the following claims.

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